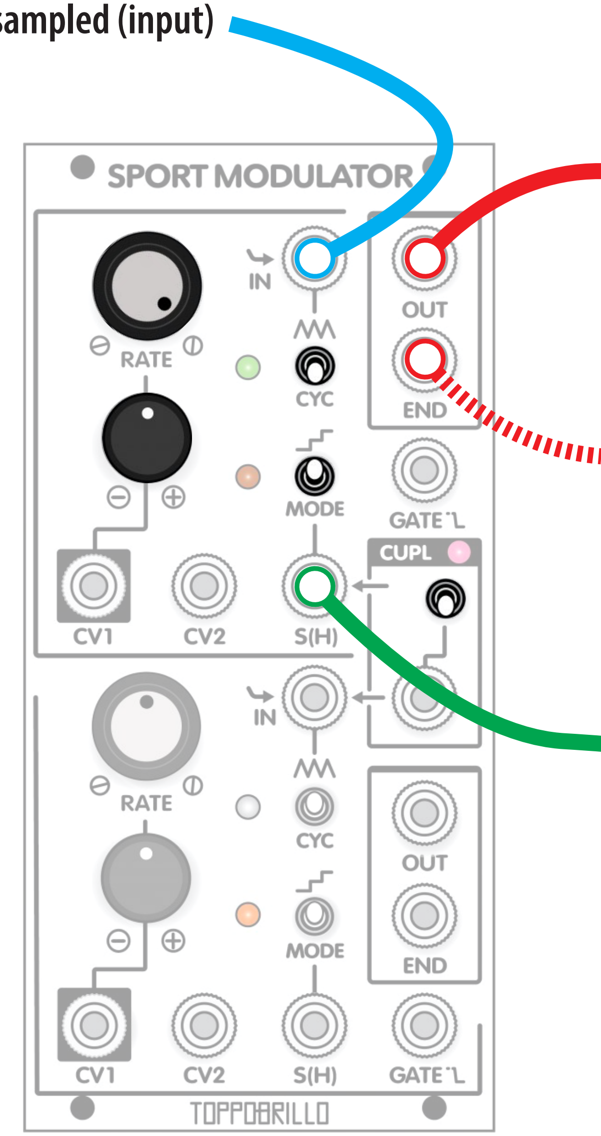
Sample & Hold

voltage to be sampled (input)

sampled, held voltage (output)

RATE will slew the incoming signal (not the output), so for conventional S&H use, RATE should be set fast (high).

Extra: there may be niche reasons to slew the input (use a lower RATE); for example, if the input signal is fluctuating wildly, and you want to average it out prior to sampling, or thin out the gates emitting from the END comparator.



outputs high (5V) when the voltage at IN is *equal or greater* to that at OUT and low (0V) if the voltage at IN is *lower* than that at OUT. Experiment.*

trigger new sample (input)

Extra: As always, if you patch a gate signal to the GATE input, the signal at IN is replaced with 0V whenever your gate signal is high (~1.5V or more). Depending on RATE, this feature can be used creatively to nullify or distort the incoming signal for sampling or the END comparator. Experiment.

*Patch idea: patch a pitch CV to IN, trigger a new sample once in a while with a clock signal, and patch END to a VCA controlling an effects send. The VCA will now close whenever the pitch at IN drops below the currently-sampled pitch.

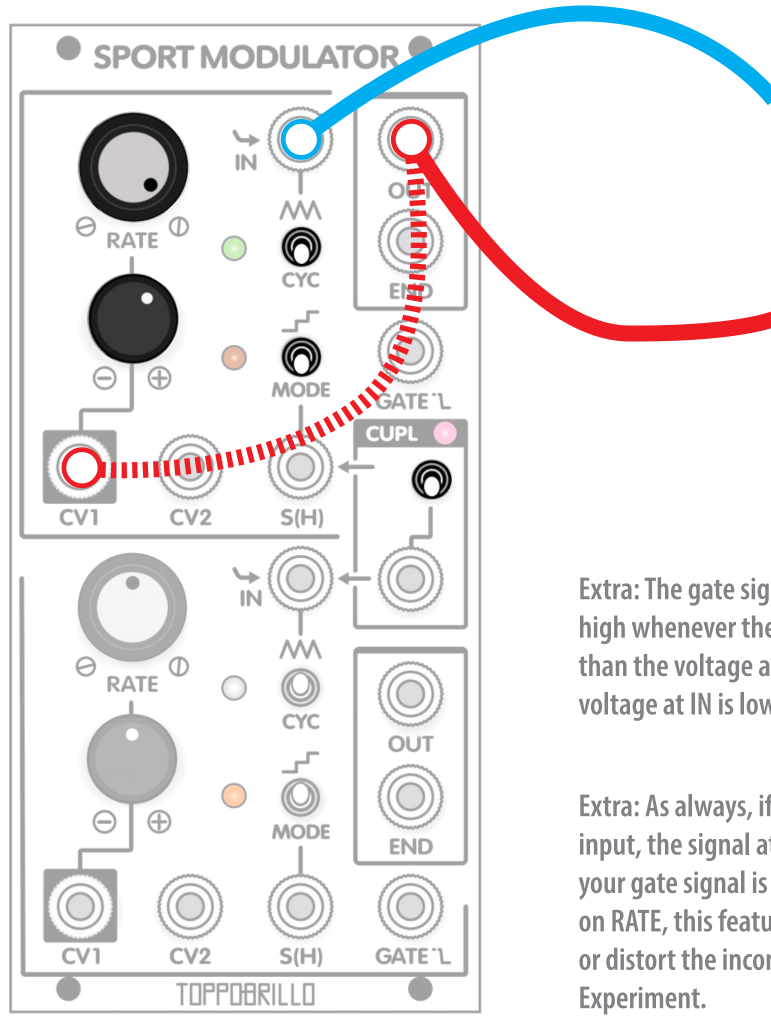
This patch requires only one half of Sport Modulator.
The other half can be employed in an identical manner, or used for another purpose.

Lag Processor / Slew Limiter

Set RATE high (fast) to pass incoming signal unaffected (no slewing).
Set RATE lower (slow) to slew (smooth it out).

Optional: patch control voltage to CV1 or CV2 to modulate the slew rate. If using CV1, adjust the attenuverter to taste. Experiment.

Optional: if you mult the OUT to CV1 and adjust the attenuverter—start at 1pm and experiment—you can achieve non-linear (curved) slewing.



voltage to be slewed

slewed output

Extra: The gate signal from the END output will be high whenever the voltage at IN is equal to or greater than the voltage at OUT, and low whenever the voltage at IN is lower than the voltage at OUT.

Extra: As always, if you patch a gate signal to the GATE input, the signal at IN is replaced with 0V whenever your gate signal is high (~1.5V or more). Depending on RATE, this feature can be used creatively to nullify or distort the incoming signal (subject to RATE). Experiment.

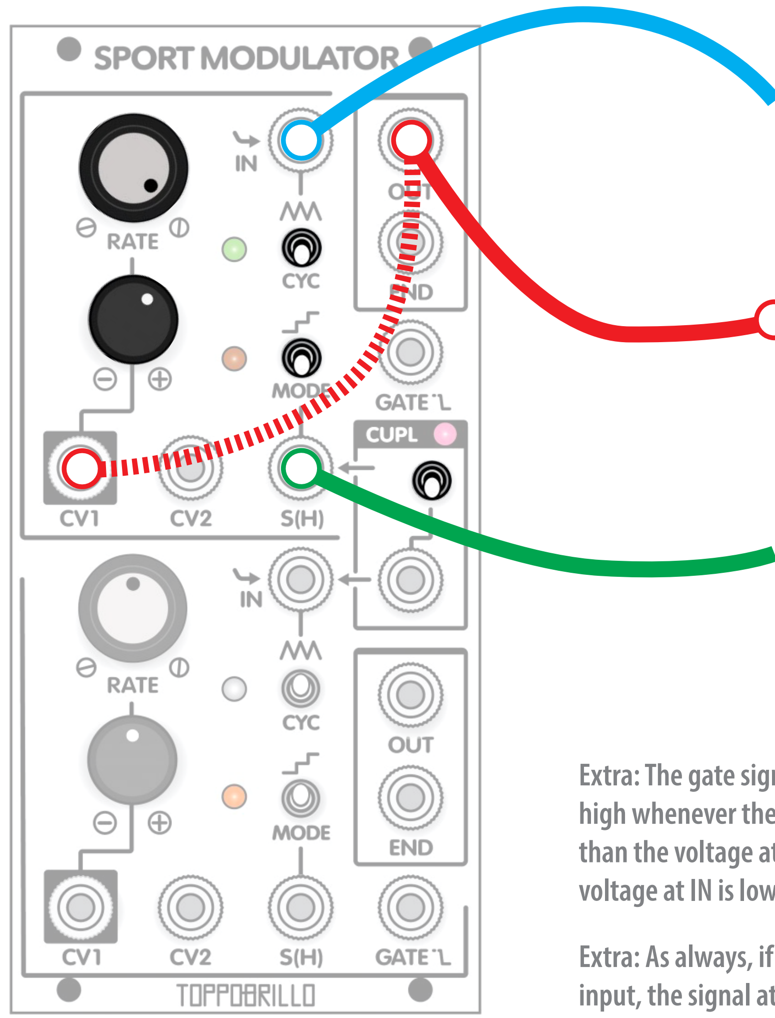
This patch requires only one half of Sport Modulator.
The other half can be employed in an identical manner, or used for another purpose.

Track & Hold / Lag & Hold

RATE will slew (lag) the incoming signal.
Set high (fast) to preserve incoming signal.
Set lower (slow) to smooth it out.
Experiment.

Optional: patch control voltage to CV1 or CV2 to modulate the slew rate. If using CV1, adjust the attenuverter to taste.

Optional: if you mult the OUT to CV1 and adjust the attenuverter (start at 1pm and experiment), you can achieve non-linear (curved) slewing.



input voltage to be tracked/slewed

output voltage

hold gate input:
high is hold (freeze output)
low is track

Extra: The gate signal from the END output will be high whenever the voltage at IN is equal to or greater than the voltage at OUT, and low whenever the voltage at IN is lower than the voltage at OUT.

Extra: As always, if you patch a gate signal to the GATE input, the signal at IN is replaced with 0V whenever your gate signal is high (~1.5V or more). Depending on RATE, this feature can be used creatively to nullify or distort the incoming signal (subject to RATE). Experiment.

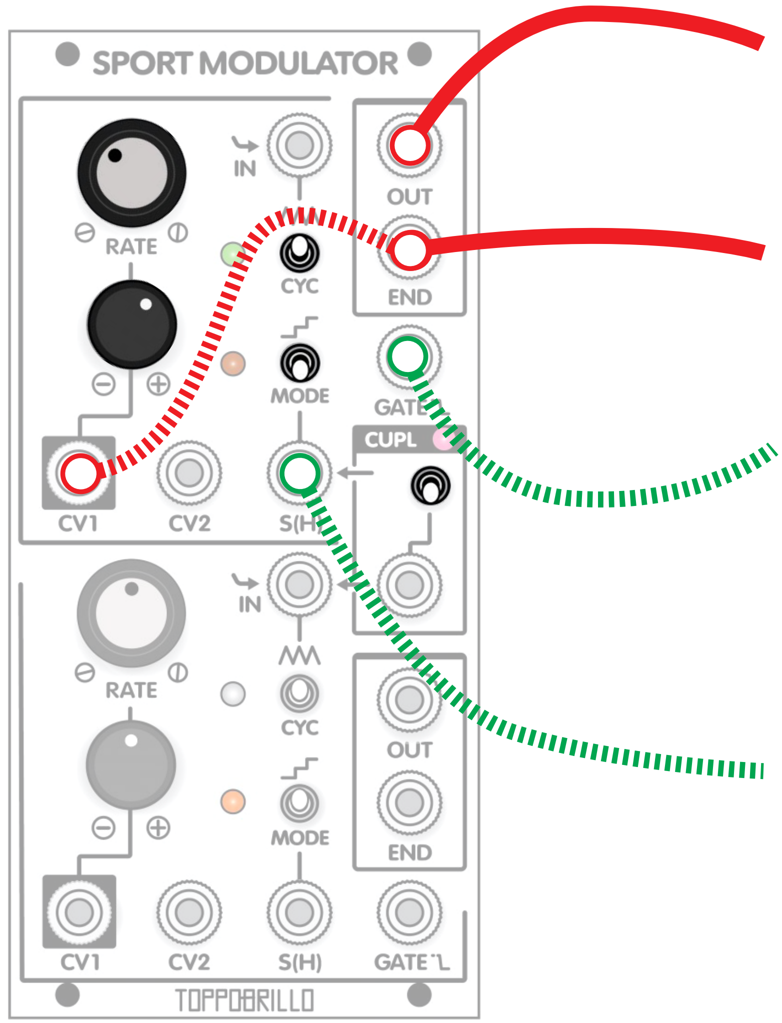
This patch requires only one half of Sport Modulator.
The other half can be employed in an identical manner, or used for another purpose.

VCLFO/clock

RATE sets the frequency of the LFO from around 0.033Hz (30 second cycle) to around 700hz.

Optional: patch control voltage to CV1 or CV2 to modulate the frequency of the LFO. If using CV1, adjust the attenuverter to taste.

Optional: if you mult END to CV1 and adjust the attenuverter one way or the other, you can skew the triangle shape of the LFO into a saw or ramp wave. Note that doing so does affect the frequency. Experiment.



output LFO (triangle)

square wave (clock) at same frequency

(Optional) VCA-like gate input:
if high, OUT is 0V, END is held
if low, OUT is LFO, END is clock

(Optional) hold gate input:
if high, OUT is held, END is held
if low, OUT is LFO, END is clock

This patch requires only one half of Sport Modulator.
The other half can be employed in an identical manner, or used for another purpose.

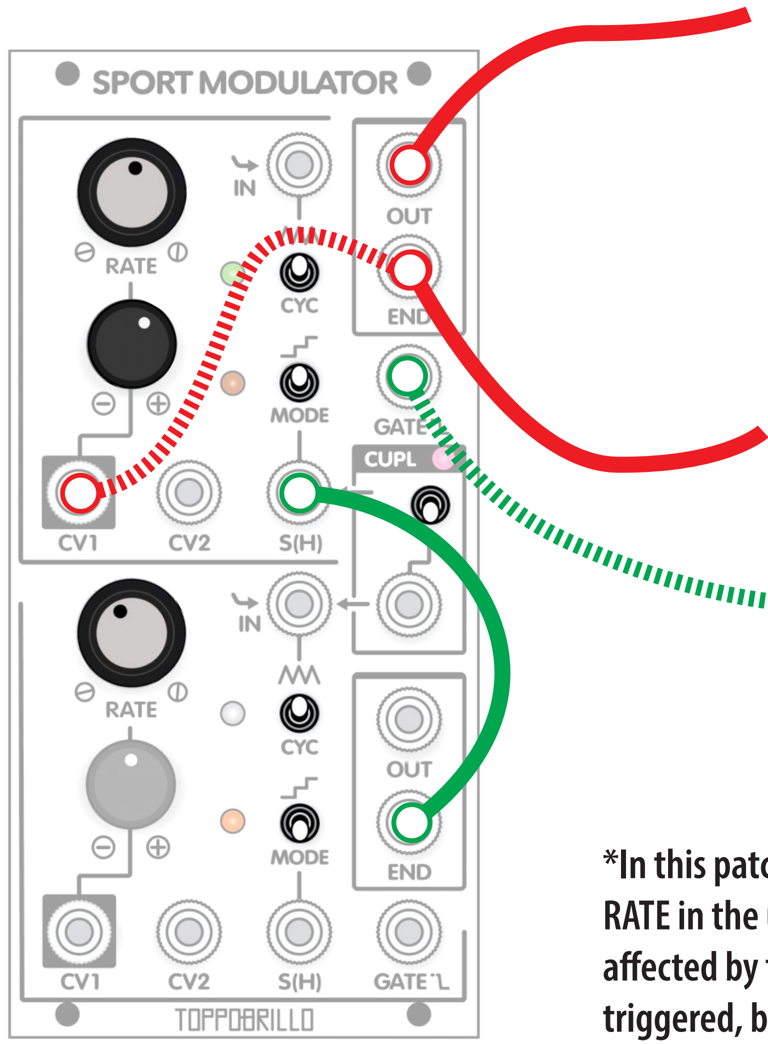
Stepped VCLFO/clock

RATE sets the base frequency of the upper LFO*

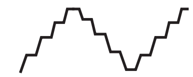
Optional: if you mult END to CV1 and adjust the attenuverter one way or the other, you can skew the triangle shape of the LFO into a saw or ramp wave. Note that doing so does affect the frequency. Experiment.

We use the lower half to generate a separate clock, patching its END to the sample input on the upper half. The RATE control for the lower half sets the frequency of that clock.

(There is no obligation to use the lower half of Sport Modulator in this patch—you could use a square wave or clock signal from elsewhere in your system.)



output LFO (stepped shape)



coarseness, length, and quantity of stepping depends on ratio of RATE and the frequency the sample input is triggered (below)

square wave (clock) at same frequency as output LFO

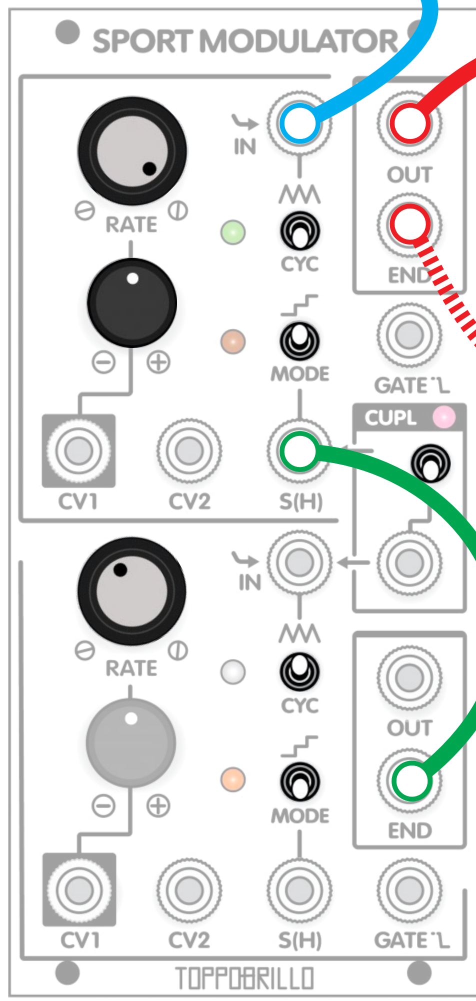
(Optional) VCA-like gate input:
if high, OUT is 0V, END is held
if low, OUT is LFO, END is clock

*In this patch, the base frequency set by RATE in the upper half will be significantly affected by the rate the sample input is triggered, because each triggering freezes the cycle, drawing it out. Experiment.

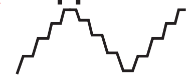
Stepped Modulation (Sample & Hold variant)

voltage to be sampled (input)

!!! This example is essentially the same as the Sample & Hold example, but uses a regular clock signal to trigger sampling. It can also generate some comparable results to the Stepped VCLFO example, but from an external voltage source rather than the internal cycling feature. See also the related Bit Crushing example.



stepped voltage (output)*



coarseness, length, and quantity of stepping depends on ratio of RATE and the frequency the sample input is triggered (below)

END is doing what it basically always does, but in this particular patch, the result is a complex rhythm that depends on the fluctuations of the voltage at IN and the rate of the clock at S(H).

As per the Stepped VCLFO example, we use the lower half to generate a separate clock, patching its END to the sample input on the upper half. The RATE control for the lower half sets the frequency of that clock.

(There is no obligation to use the lower half of Sport Modulator in this patch—you could use a square wave or clock signal from elsewhere in your system.)

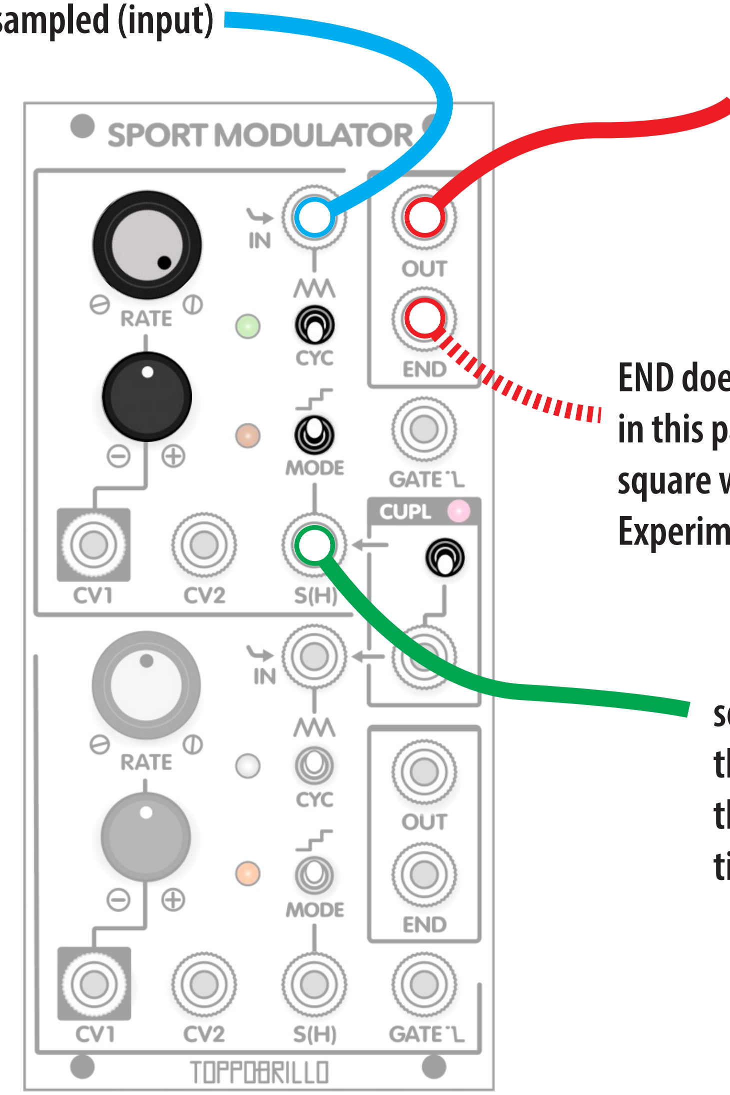
*Patch idea: patch OUT to the 1v/o of an oscillator (optionally, first through a pitch quantizer) for an arpeggio-like effect that varies depending on the voltage fluctuations at IN and the rate of the clock at S(H).

“Bit Crushing” (Sample & Hold Variant)

audio be sampled (input)

crushed/distorted audio (output)

RATE will act as a kind of low pass filter on the input signal



END does basically what it always does, but in this particular patch the result is a gnarly square wave approaching noise. Experiment.

!!! This example is essentially the same as the Sample & Hold example and the Stepped Modulation example, but processes audio and employs an audio-rate signal to trigger sampling.

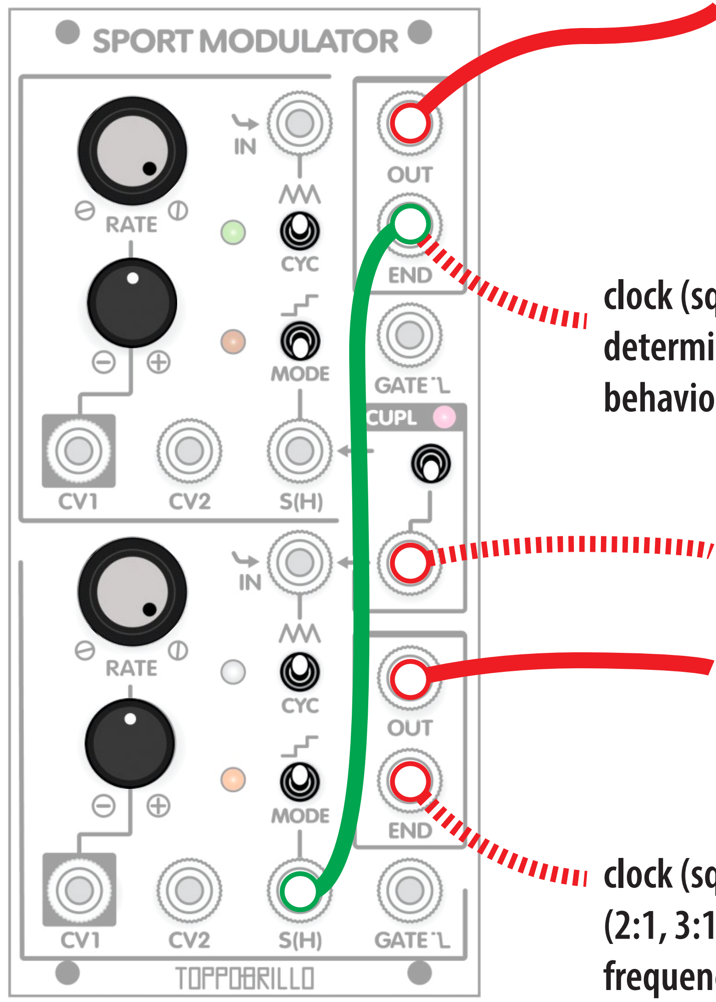
square wave from an oscillator; adjust the frequency of the oscillator to alter the degree of “bit crushing” and related timbres

This patch requires only one half of Sport Modulator.
The other half can be employed in an identical manner, or used for another purpose.

Synchronized Cycling Modulations (Smooth and Stepped)

As per the plain VCLFO example, top half RATE sets the cycling frequency of the top half.

Bottom half RATE sets the ratio (2:1, 3:1, 4:1, etc.) relative to the top half that the bottom half cycles.



triangle LFO output at frequency determined by top half RATE (normal VCLFO behavior)

clock (square wave) output at frequency determined by top half RATE (normal VCLFO behavior)

complex gate pattern (a bit like morse code)

stepped LFO output at ratio (2:1, 3:1, 4:1, etc.) of top half frequency

clock (square wave) output at ratio (2:1, 3:1, 4:1, etc.) of top half frequency

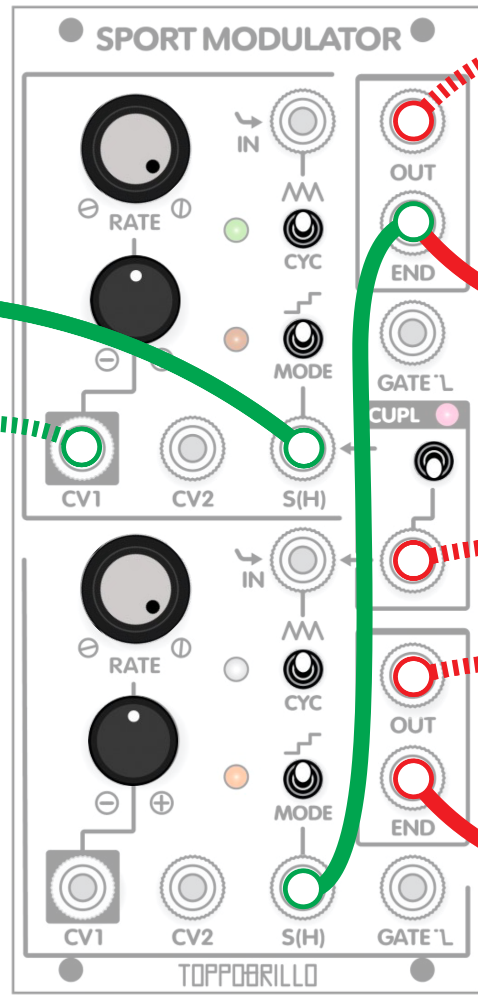
VC divider & Sub-oscillator (the old Sport Mod v1 way)

Upper half RATE sets the ratio (2:1, 3:1, 4:1, etc.) relative to the clock at S(H). Start with RATE fully clockwise (2:1).

clock (e.g., square wave) input

(optional) CV control over ratio

You can use only one half of Sport Modulator as a divider, but we are showing here how you can clock the second half with the END of the first to *subdivide the subdivision,* and to get weird gates from the comparator. If you do, the bottom half RATE sets the ratio (2:1, 3:1, 4:1, etc.) relative to the top half. Start with RATE fully clockwise (2:1).



output LFO (stepped shape)

period depends on divided ratio

clock (square wave) output at divided frequency of S(H) input

weird gate stream (experiment)

output LFO (stepped shape)

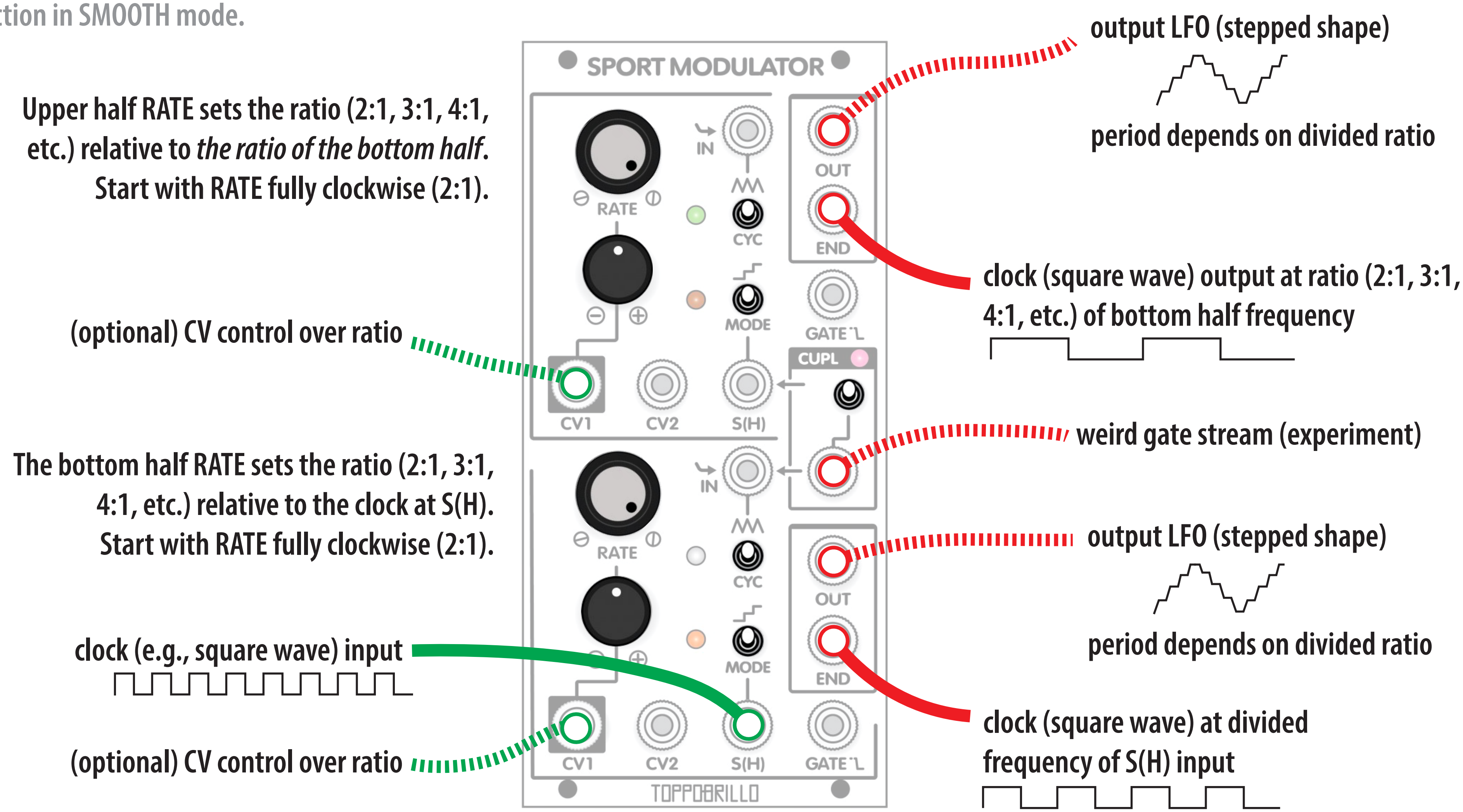
period depends on divided ratio

clock (square wave) output at ratio (2:1, 3:1, 4:1, etc.) of top half frequency

Note: this patch basically works as an audio-rate sub-oscillator, but you may find it a bit buzzy, tweaky, and unstable.

VC divider & Sub-oscillator (the new Sport Mod v2 way)

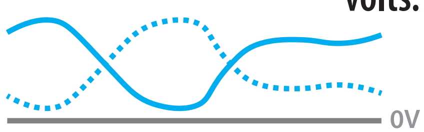
Flipping the CUPL switch up "couples (via normalization) the COMPARATOR output (20V p-p internally) to both the TOP section's S(H) input as well as the BOTTOM section's INPUT. It also locks the TOP section in STEPPED mode and the BOTTOM section in SMOOTH mode.



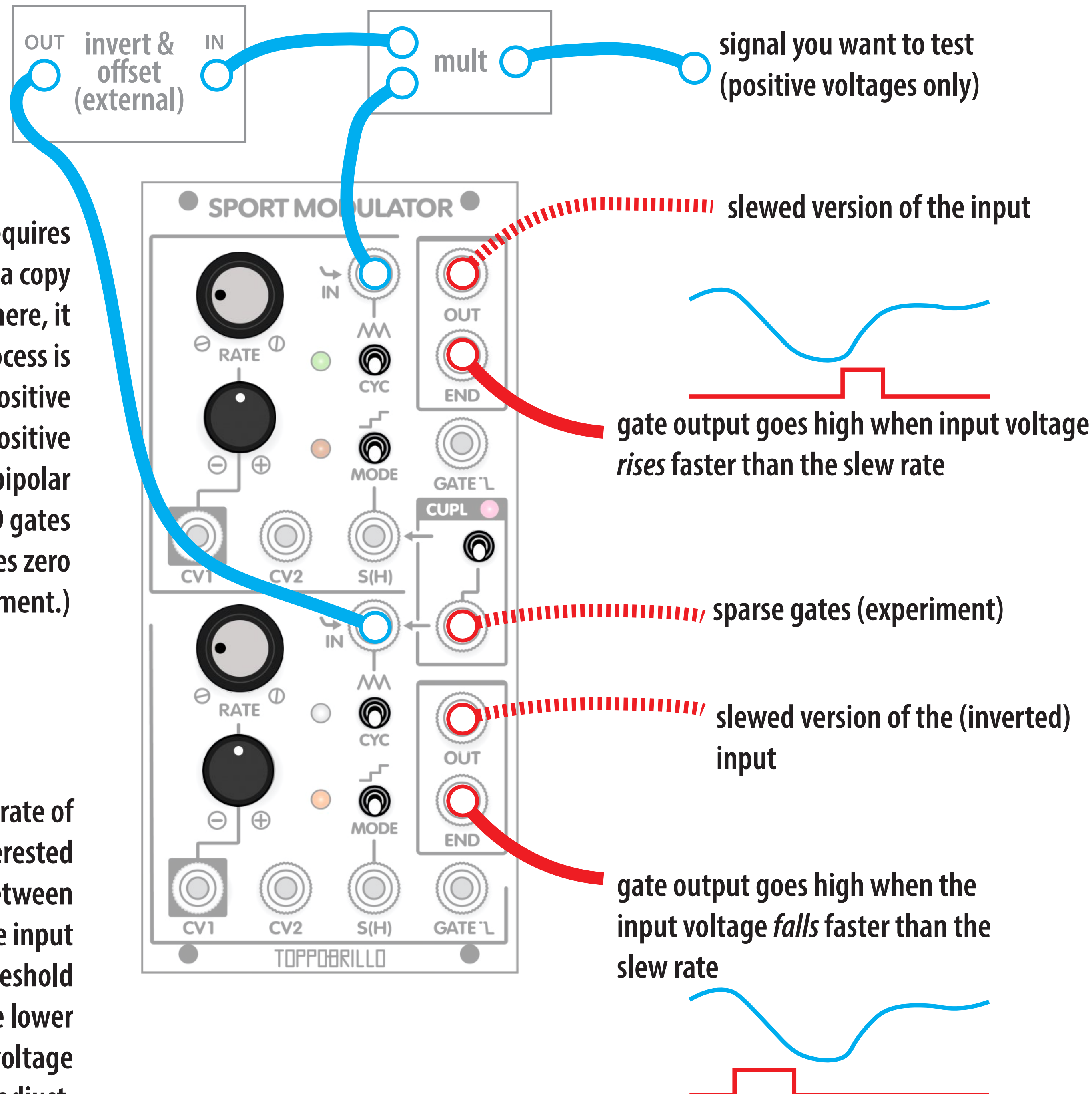
Note: this patch basically works as an audio-rate sub-oscillator, but you may find it a bit buzzy, tweaky, and unstable.

Slope detector

This is a simple enough patch, but it requires that you be able to invert and offset a copy of your input signal. Also, as written here, it presumes the signal you wish to process is unipolar—the top copy is only positive voltage *and* the bottom copy is only positive voltage. (The patch "still works" with bipolar voltage, but you will find that the END gates invert on you when your input crosses zero volts. Experiment.)



As usual, RATE determines the slew rate of the input, but in this case we are interested in how it establishes a threshold between slow changes and fast changes in the input signal. The upper RATE sets the threshold for rising voltage speed, and the lower RATE sets the threshold for falling voltage speed. Start both at 9 o'clock, and adjust.

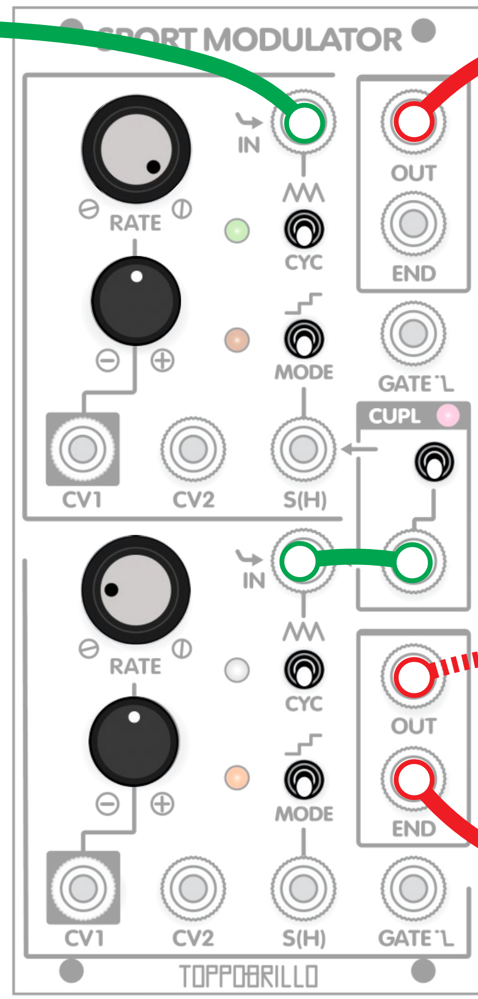


“Autolag” sequencing a la Buchla MARF

CV input from step sequencer, typically a pitch CV

Upper half RATE will slew the pitch, adding portamento (start at fully CW for no slew)

The bottom half RATE effectively controls the overall rate of the sequence, but is controlling the slew rate between the high and low states of the comparator signal (start at 9pm and adjust)



CV output (e.g., pitch to oscillator)

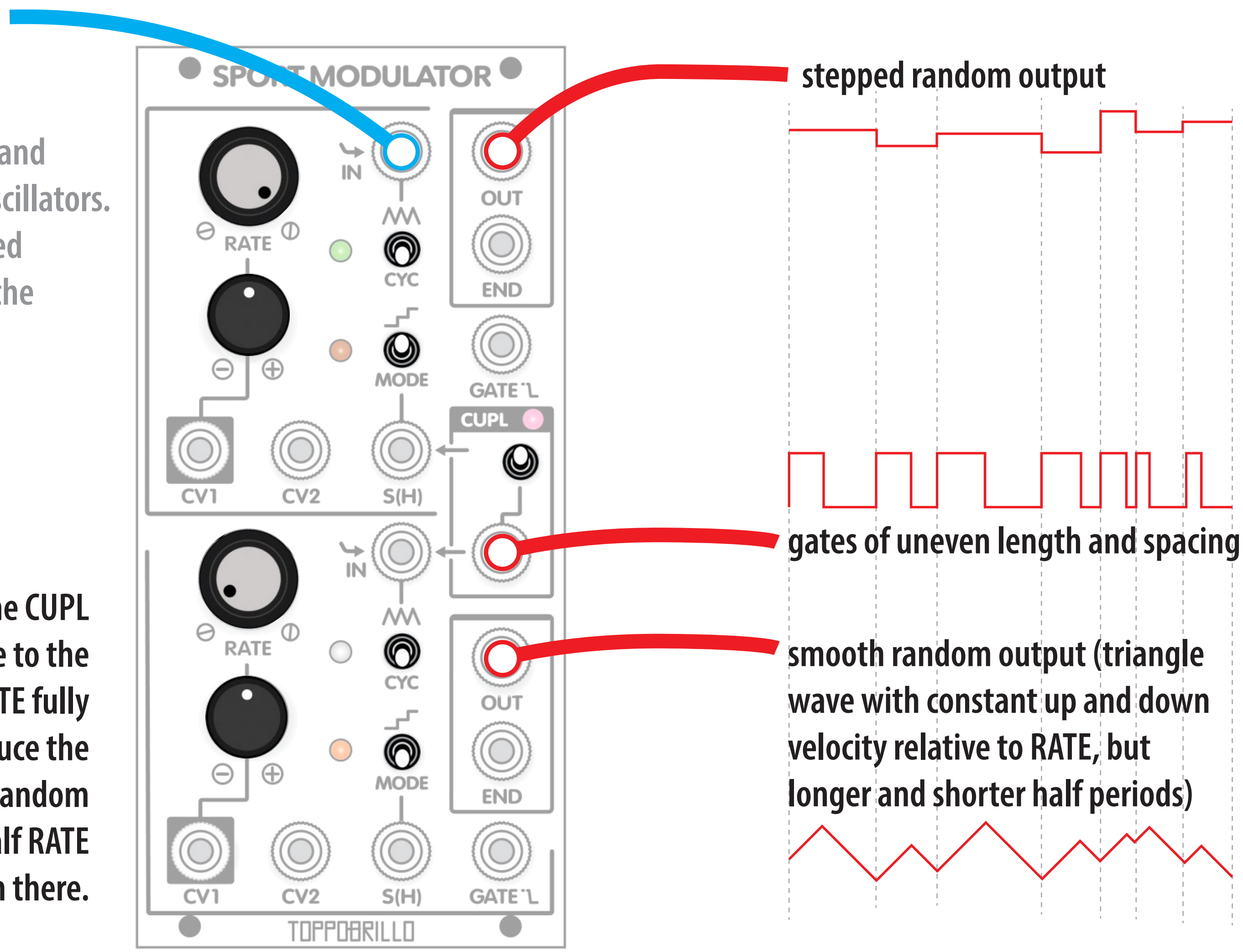
triangle LFO-like output, but with varying periodicity (can make an interesting pitch or mod source—experiment)

(variable length) clock/gates to advance the step sequencer (and optionally send to an envelope generator)

!!! In this patch, upward pitch changes will slow the progression of the sequence, and downward pitch changes will speed it up. It is crucial to experiment with the sequence while it is playing.

Serge Random Source Patch

Extra: experiment with colored noise and other types of signals, such as from oscillators. Note that the amplitude of the stepped random output is strongly related to the amplitude of the input source.



For this patch, you simply flip the CUPL switch up and connect a noise source to the top half IN. Set the top half RATE fully clockwise (lowering will simply reduce the amplitude of your stepped random output). Start with the bottom half RATE around 8pm and adjust from there.

Extra: if you want truly “smooth” random output, pass it through another slew.

“Digital” oscillator

noise source, oscillator or other input

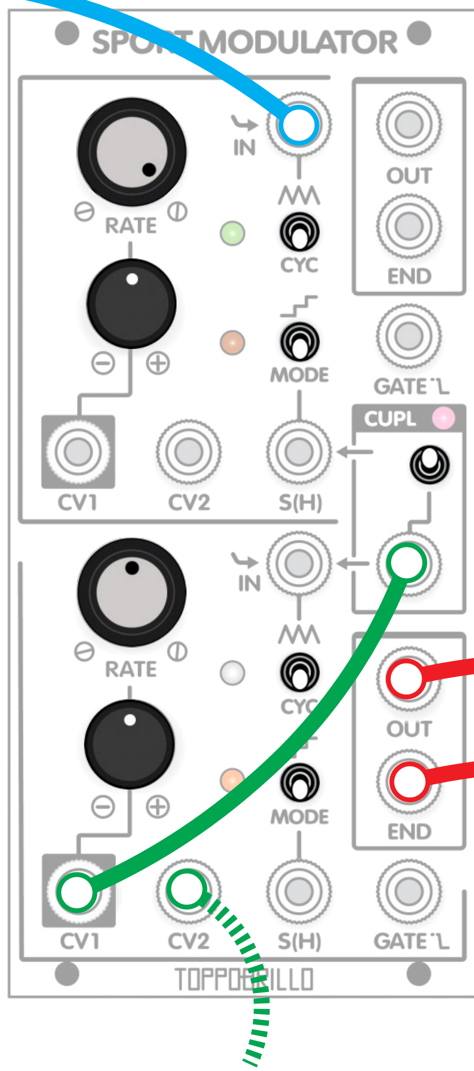
Alternatively, just flip the CYC switch up on the top half to use the top half as the modulation oscillator for the comparator

Start with top half RATE fully CW; reducing RATE with a source at IN will attenuate its effect on the comparator

If CYC is enabled for top half, then RATE sets the frequence of top half oscillation, as always

Bottom RATE controls frequency (pitch)

Patching the comparator output to bottom CV1 yields a wide range of timbral effects across small adjustments of the associated attenuverter



optional pitch CV
(does not track 1V/Oct)

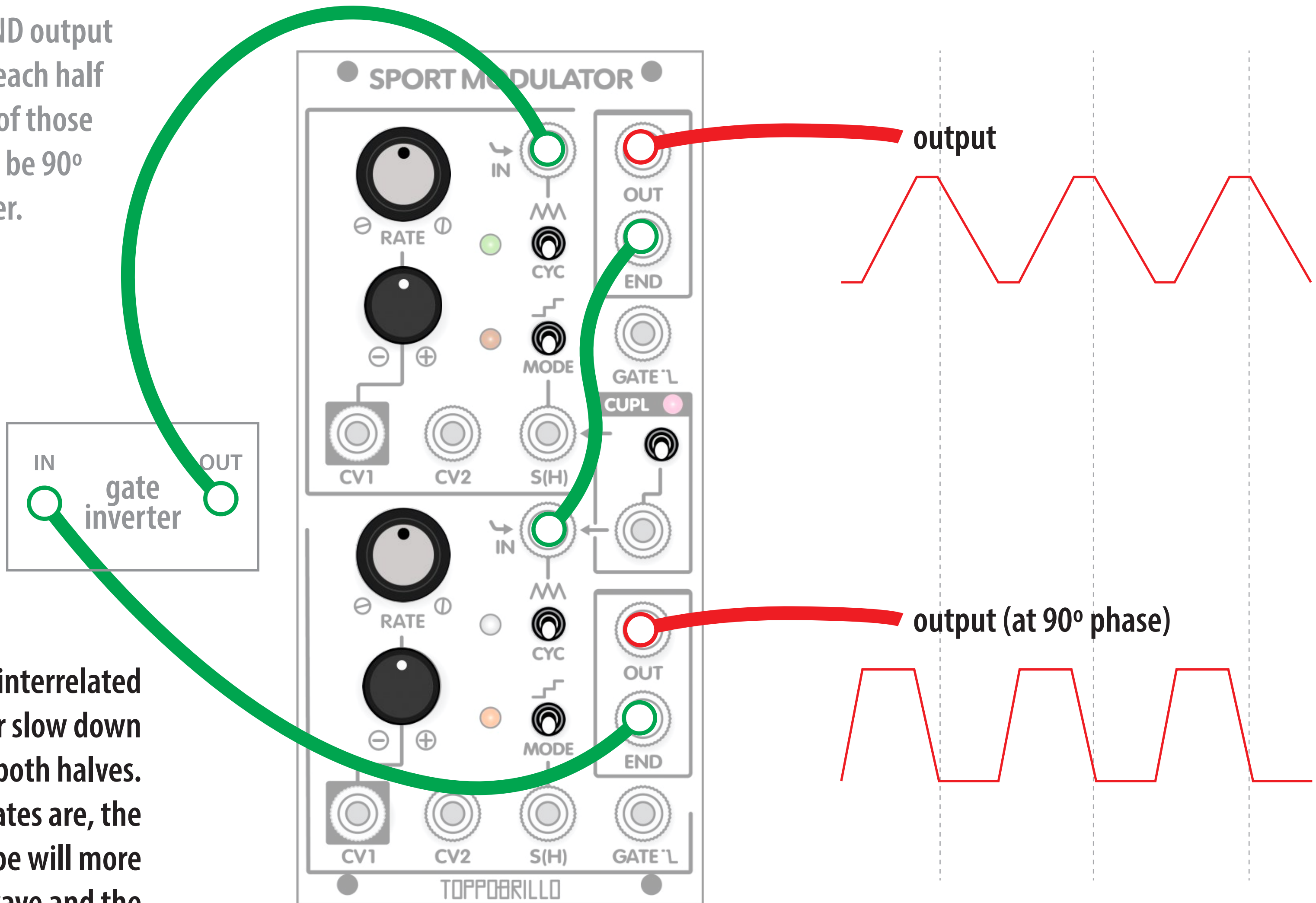
The principle of this patch is that, with CUPL engaged, the lower half is oscillating, but driven by the state of the comparator, which can be influenced by whatever the top half is doing.

audio out (modulated triangle wave)

audio out (modulated square wave)

Simple Quadrature Patch

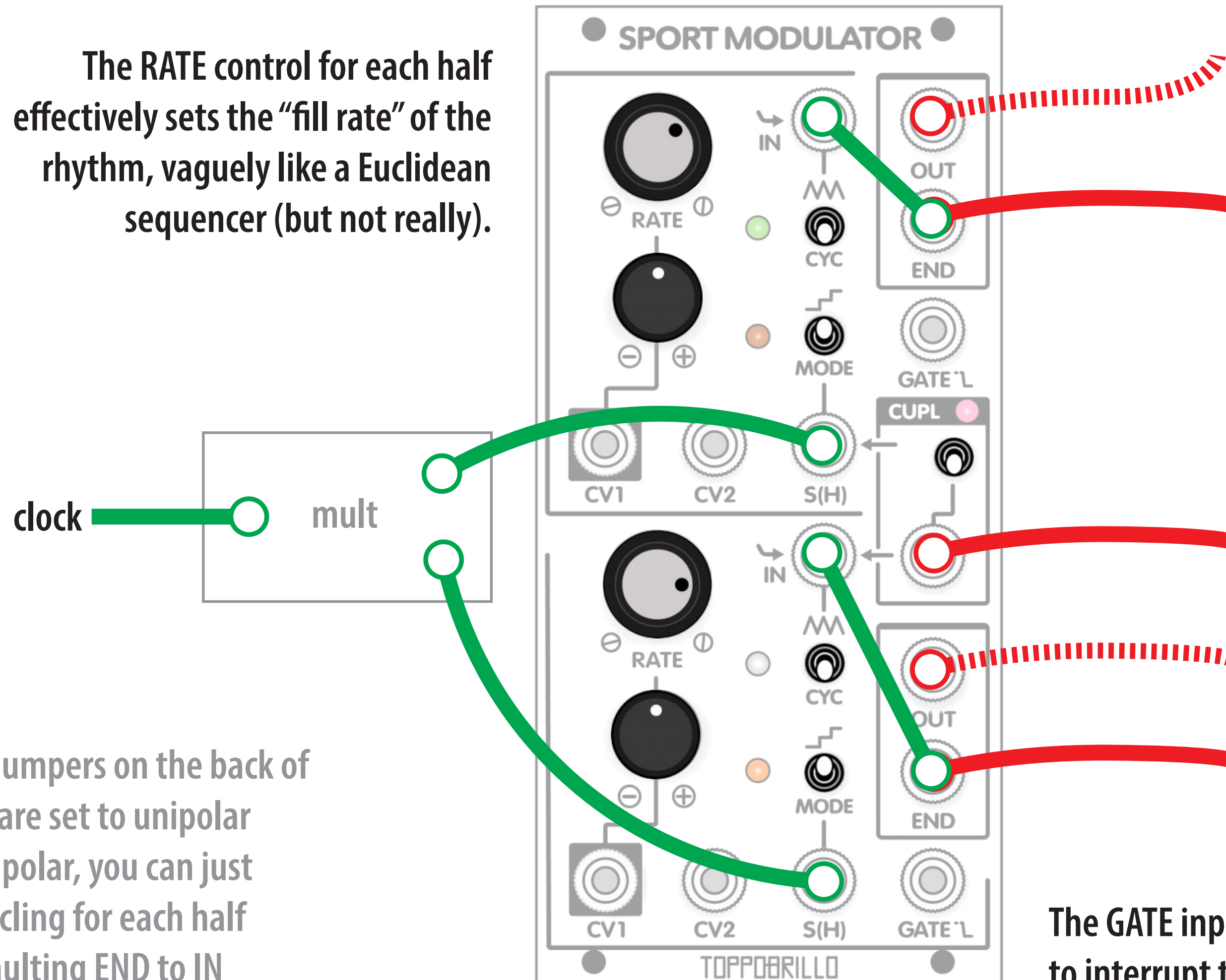
The principle of this patch is that each half is slewing the END output of the other, and causing each half to cycle. By inverting one of those END outputs, one half will be 90º out of phase with the other.



Both RATE controls are interrelated and will speed up or slow down the overall cycling of both halves. The further apart the rates are, the faster wave shape will more resemble a square wave and the slower a triangle wave.

Triple Rhythm Generator

The RATE control for each half effectively sets the “fill rate” of the rhythm, vaguely like a Euclidean sequencer (but not really).



potentially useful stepped modulation signal–patch to timbre on drum modules and/or patch to CV1 of either half and annuvert for additional rhythmic variations

rhythm A

rhythm C

potentially useful stepped modulation signal (see above)

rhythm B

The GATE inputs on either half can be used to interrupt the associated rhythm.

Note: if the jumpers on the back of the module are set to unipolar instead of bipolar, you can just switch on cycling for each half instead of multing END to IN

Patch developed by grrrwaaa and Naive Teen Idol on MW